海奇半导体

B200

Brief Datasheet

HI-CHIP Corporation

B200

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B200 Brief Data Sheet

1 What is B200

The HC B200 is a cost effective, single-chip solution for high definition multimedia applications. The B200 contains a 32bit RISC CPU and rich peripherals. The general-purpose peripherals include USB EHCI Host/Device, TV encoder, Audio DAC, SD/MMC ,SPI NAND and SPI NOR , DDR2 or DDR3 and so on. The chips build-in a multi-format video decoder, a 2D graphic accelerator, a high quality display engine and a flexible audio DMA engine. The whole chip provides high system performance and can satisfy a wide variety of video and audio applications.

2 Features of B200

2.1 Key Specification

- Accelerator for MPEG and H.264 decoding with high definition solutions, max 1920x1080p@60
- 2-ports USB EHCI Host/Device, one can support OTG
- RGB888 interface
- 16-bit DDR2 or DDR3

2.2 Power down Control

- 3.3V/1.8V/1.5V/1.1V Power supply
- Power save mode for every module

2.3 High-Performance CPU

- 32-bit RISC
- Maximum frequency of 800Mhz, applications smoothly
- Independent I-cache, D-cache

2.4 Memory and Bus Interfaces

- Extra 16-bit DDR2/DDR3 DRAM interface
    - DDR2 frequency up to 1066M

- DDR33 frequency up to 1333M
- Max 256 MB capacity

- Suppor1- or 2-bit SPI-FLASH :Maximum capacity of 32 MB

2.5 Video Decoding

- H.264 BP/MP/HP@level 5.0, 1080p@60 fps
- H264 MVC, 1080p@60 fps
- MPEG1, 1080p@60 fps
- MPEG2 SP@ML, MP@HL, and 1080p@60 fps
- MPEG4 SP@level 0−3, ASP@level 0−5, GMC, 1080p@60 fps
- MPEG4 short header format (H.263 baseline), 1080p@60 fps
- DivX 3/4/5/6, 1080p@60 fps
- AVS baseline@level 6.0, AVS+(AVS-P16), and 1080p@60 fps
- VC-1 SP@ML, MP@HL, and AP@level 0−3, 1080p@60 fps

2.6 Image Decoding

- JPEG hardware decoding, a maximum of 64 megapixels
- Supported formats of 400, 420, 411, 422, 422T, and 444
- MJPEG baseline decoding
- Gray-scale image, true color image, indexed-color image,
- gray-scale image with alpha channel data, and true color
- image with alpha channel data

2.7 2D Graphics Acceleration

- Hardware acceleration engine, supporting highly efficient 2D processing
- Data formats of ARGB, CLUT, and AYCbCr
- Copying, filling, pattern filling, resizing, clipping, alpha blending, colorkey, and clip mask
- ROP
- Anti-flicker, gamma correction, and contrast/luminance adjustment
- Programmable scanning mode
- Linked-list operation

2.8 Audio Encoding/Decoding

- Audio decoding formats
  - Dolby Digital, Dolby Digital Plus, Dolby TrueHD
  - DTS, DTSHD
  - MPEG L1/L2
  - MP3
  - AAC_LC, HE_AAC, HE_AACV2
  - LPCM
  - APE
  - FLAC
  - OggVorbis
  - AMRNB
  - AMRWB
  - G.711 (u/a)
- Audio encoding formats
  - AAC_LC, HE_AAC, HE_AACV2
  - AMR-NB
  - G.711 (u/a)

2.9 Audio Interface

- S/PDIF output support
- I2S output support
- 2-Channel Embedded Audio DAC for stereo output
- Support I2S input for MIC

2.10 Video Interface

- One RGB interface
- Support 656 input

2.11 Peripheral Interfaces

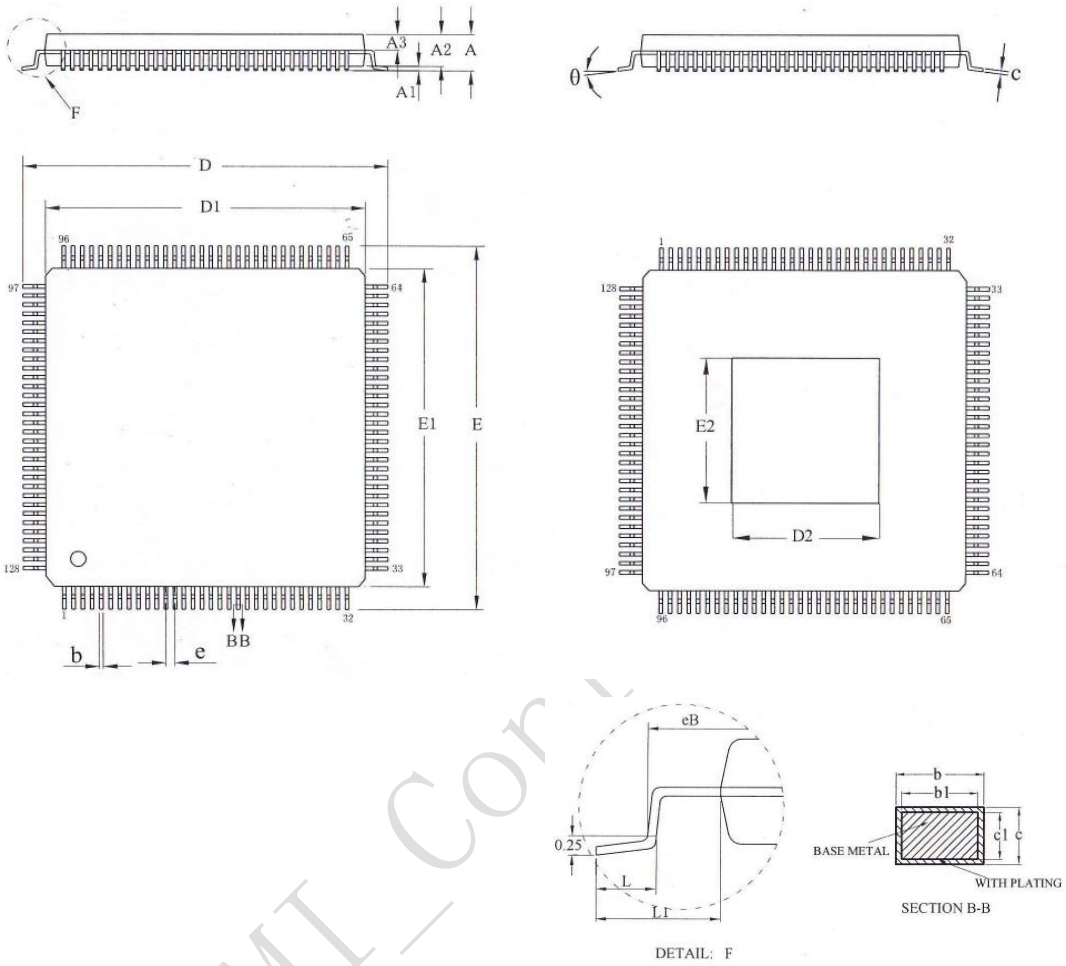
- One USB 2.0 OTG ports and One USB2.0 Host/Device(SW select)
- One SDIO 2.0 interface, supporting 3.3 V component

- One IR receiver
- Multiple I2C interfaces
- UART interfaces
- SPI interface
- Multiple GPIO interfaces
- PWM interfaces

2.12 Others

- 2-layer PCB
- Various boot modes
- Boot program download and execution over a serial port
- Low-power design technologies

3 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	—	0.22
b1	0.13	0.16	0.19
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	—	15.35
e	0.40BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	7°

L/F Size (mil) \ Size (mm)	D2	E2
218*218	4.95REF	4.95REF